REMARKS

The Office Action of January 18, 2008, has been received and reviewed.

Claims 1-39 and 41-67 are currently pending in the above-referenced application. Of these, claims 1-13, 17-26, 31-33, 35-39, and 42-44 are currently under examination (claims 35 and 36 apparently having been returned to consideration). Each of claims 1-13, 17-26, 31-33, 35-40, and 42-44 stands rejected. Claim 40 was previously canceled without prejudice or disclaimer, rendering the rejection of that claim moot. Claims 14-16, 27-30, 34-36, 41 and 45-67 were withdrawn from consideration following elections made in response to restriction and species election requirements.

Reconsideration of the above-referenced application is respectfully requested.

Rejections under 35 U.S.C. § 102

Claims 1-10, 17, 19-26, 33, and 35-40 have been rejected under 35 U.S.C. § 102.

A claim is anticipated only if each and every element, as set forth in the claim, is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Nakanishi

Claims 1-10, 17, and 19 were rejected under 35 U.S.C. § 102(e) for reciting subject matter which is purportedly anticipated by that described in U.S. Patent Application Publication 2001/0013643 of Nakanishi et al. (hereinafter "Nakanishi").

Independent claim 1 is drawn to a semiconductor device that includes a semiconductor die and a dielectric spacer. The distance that the dielectric spacer protrudes from a surface the semiconductor die will accommodate a height of at least one intermediate conductive element. More specifically, as amended and presented herein, independent claim 1 recites that the distance that the dielectric spacer protrudes from the surface of the semiconductor die will accommodate an intermediate conductive element that "includes a bonding portion secured to a contact of the

semiconductor die and a laterally extending portion located between and electrically isolated from an active surface of the semiconductor die and a back side of the adjacent semiconductor die." Additionally, voids in the dielectric spacer communicate with a lateral periphery of the dielectric spacer.

In the semiconductor device assembly shown in FIG. 9 of Nakanishi, there are no bond wires 8 with portions that extend between semiconductor devices 1 and 2 or between semiconductor devices 3 and 4. Therefore, it is evident from FIG. 9 of Nakanishi that Nakanishi does not expressly or inherently describe a semiconductor device with a dielectric spacer layer that accommodates an intermediate conductive element with "a bonding portion secured to a contact of [a] semiconductor die and a laterally extending portion located between and electrically isolated from an active surface of the semiconductor die and a back side of [an] adjacent semiconductor die...," as would be required for Nakanishi to anticipate each and every element of amended independent claim 1 under 35 U.S.C. § 102(e).

Each of claims 2-10 and 17 is allowable, among other reasons, for depending directly or indirectly from claim 1, which is allowable.

Claim 5 is also allowable since Nakanishi lacks any express or inherent description that the polyimide spacer 24 thereof may have a thickness that exceeds a height that at least one intermediate conductive element (*e.g.,* bond wires 8a, 8b of FIG. 9) protrudes above the active surface of a semiconductor device 2, 3 to which the polyimide spacer is secured.

Claim 8 is additionally allowable because Nakanishi does not expressly or inherently describe that the polyimide spacer 24 thereof comprises a pattern.

Claim 9 is further allowable since Nakanishi includes no express or inherent description that the polyimide spacer 24 thereof comprises randomly arranged features.

Claim 17 is also allowable because Nakanishi does not expressly or inherently describe that adhesive material may be present on an exposed surface of the polyimide spacer 24.

Independent claim 19 is drawn to a semiconductor device assembly that includes, among other things, a nonconfluent spacer layer that spaces an active surface of a first semiconductor

device apart from a back side of a second semiconductor device. Thus, the active surface of the first semiconductor device faces the back side of the second semiconductor device.

Nakanishi does not expressly or inherently describe an assembly in which the back side of one semiconductor device faces the active surface of another semiconductor device. Rather, the description of Nakanishi is limited to assemblies in which the active surfaces 1a and 2a, 3a and 4a of stacked pairs of semiconductor devices 1 and 2, 3 and 4 face each other. *See, e.g.*, Fig. 9; paragraphs **[0077]** and **[0047]**. Therefore, Nakanishi does not anticipate the subject matter recited in independent claim 19. Therefore, under 35 U.S.C. §§ 102(e), the subject matter recited in independent claim 19 is allowable over the subject matter disclosed in Nakanishi.

Withdrawal of the 35 U.S.C. § 102(e) rejections of claims 1-10, 17, and 19 is respectfully requested, as is the allowance of each of these claims.

Foster

Claims 19, 22-26, 33, and 35-40 stand rejected under 35 U.S.C. § 102(e) for being directed to subject matter that is purportedly anticipated by the subject matter described in U.S. Patent 6,437,449 of Foster (hereinafter "Foster").

Claims 35 and 36 were previously withdrawn from consideration. Clarification of the status of both of these claims is respectfully requested.

Claim 40 has been canceled without prejudice or disclaimer, rendering the rejection of that claim moot.

With respect to the subject matter to which independent claim 19 is directed, it its respectfully submitted that Foster provides no express or inherent description of a semiconductor device assembly that includes a "non-confluent spacer layer."

The term "confluent" means "flowing or running together, blending into one..." Dictionary.com Unabridged (v. 1.1) (Random House 2006). A confluent spacer would be solid within the entire confines of its outer periphery, as are the spacer layers 116 and 216 described in Foster. While it is recognized that outer peripheries of the spacer layers 116 and 216 of Foster do not extend completely to the outer periphery of either semiconductor devices 140, 108 the

disclosed assemblies, Foster does not expressly or inherently describe that there is any lack of confluency within the confines of the outer peripheries of the spacer layers 116 and 216. Thus, Foster does not expressly or inherently describe that either spacer layer 116 or spacer layer 216 is nonconfluent, as would be required for Foster to anticipate each and every element of independent claim 19 under 35 U.S.C. § 102(e).

Each of claims 22-26, 33, and 35-39 is allowable, among other reasons, for depending directly or indirectly from Foster, which is allowable.

Claim 22 is further allowable because Foster includes no express or inherent description that either spacer layer 116 or spacer layer 216 includes a plurality of laterally discrete spacers.

Claim 26 is additionally allowable since Foster does not expressly or inherently describe a semiconductor device assembly in which a nonconfluent spacer has a thickness that spaces first and second semiconductor devices 140 and 108 apart from one another a distance that is about the same as or less than a height that an intermediate conductive element (*e.g.*, wire 124, 224) protrudes above the active surface of the lower semiconductor device 108.

Claim 33 is also allowable since Foster neither expressly nor inherently describes that either spacer layer 116 or spacer layer 216 comprises a pattern.

Claim 36 is additionally allowable because Foster lacks any express or inherent description that either spacer layer 116 or spacer layer 216 is secured to semiconductor devices 140 and 108 with an adhesive material that is located within voids of the spacer layer 116, 216.

Vindasius

Claims 1-10, 17, 19-26, 33, and 37-39 have been rejected under 35 U.S.C. § 102(b) for being drawn to subject matter that is assertedly anticipated by the description provided by U.S. Patent 6,098,278 of Vindasius et al. (hereinafter "Vindasius").

The semiconductor device assembly described in Vindasius includes two semiconductor devices 150 and 152 that are arranged in a flip-chip fashion (*i.e.*, their active surfaces face one another). Col. 13, lines 1-16 and 14-15; FIGs. 14 and 15. The semiconductor devices 150 and 152 are electrically connected to one another by way of structures that include conductive

epoxy 160-coated glass spheres 162. Col. 13, lines 8-9 and 15-17; FIGs. 14 and 15. The assembly also includes wire bonds 156 that electrically connect the lower semiconductor device 152 to a lead frame 154. Col. 13, lines 6-7 and 19-21; FIGs. 14 and 15. While Vindasius purports that the glass spheres 162 define the distance between the opposed active surfaces of the semiconductor devices 150 and 152 (col. 13, lines 9-11 and 18-19), it is apparent from FIGs. 14 and 15 that the conductive epoxy 160 that coats the glass spheres 162 is also partially responsible for the distance between the semiconductor devices 150 and 152.

As the conductive epoxy 160-coated glass spheres 162 of Vindasius serve as conductive elements, they cannot be considered to comprise a "dielectric spacer layer," as would be required for Vindasius to anticipate each and every element of independent claim 1.

Furthermore, it is apparent from FIGs. 14 and 15 that no portion of any wire bond 124 extends between the semiconductor devices 150 and 152. Nor does Vindasius expressly or inherently describe a semiconductor device with a spacer layer that would accommodate a portion of a wire bond 124 or any other discrete conductive element with a laterally extending portion located between two semiconductor dice, as would be required for Vindasius to anticipate each and every element of independent claim 1.

It is also respectfully noted that independent claim 19 requires that the active surface of a first semiconductor device and the back side of a second semiconductor device face one another. In the assembly described by Vindasius, however, the active surfaces of both semiconductor devices 150 and 152 face each other. Therefore, Vindasius does not anticipate each and every element of independent claim 19.

Since Vindasius does not anticipate each and every element of independent claim 1 or independent claim 19, it is respectfully submitted that, under 35 U.S.C. § 102(b), both of these claims are drawn to subject matter that is allowable over the subject matter described in Vindasius.

Each of claims 2-10 and 17 is allowable, among other reasons, for depending directly or indirectly from independent claim 1, which is allowable.

Claim 6 is also allowable since Vindasius provides no express or inherent description of a semiconductor device in which a dielectric spacer layer protrudes from a surface of a

semiconductor die about the same distance as or a lesser distance than a discrete conductive element with a laterally extending portion protrudes above the surface of the semiconductor die.

Claim 9 is additionally allowable because Vindasius does not expressly or inherently describe a dielectric spacer layer that comprises randomly arranged features.

Claims 20-26, 33, and 37-39 are each allowable, among other reasons, for depending directly or indirectly from independent claim 19, which is allowable.

It is respectfully requested that the 35 U.S.C. § 102 rejections of claims 1-10, 17, 19-26, 33, and 35-40 be withdrawn and that each of claims 1-10, 17, 19-26, 33, and 35-39 be allowed.

Rejections under 35 U.S.C. § 103(a)

Claims 11-13, 18, 31, 32, and 42-44 have been rejected under 35 U.S.C. § 103(a).

There are several requirements in establishing a *prima facie* case of obviousness against the claims of a patent application. All of the limitations of the claim must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 985 (CCPA 1974); *see also* MPEP § 2143.03. Even then, a claim "is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR Int'l Co. v. Teleflex Inc.*, 82 USPQ2d 1396 (2007). The Office must also establish that one of ordinary skill in the art would have had a reasonable expectation of success that the purported modification or combination of reference teachings would have been successful. *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986). There must also be "an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR* at 1396. That reason must be found in the prior art, common knowledge, or derived from the nature of the problem itself, and not based on the Applicant's disclosure. *DyStar Textilfarben GmbH & Co. Deutschland KG v. C. H. Patrick Co.*, 464 F.3d 1356, 1367 (Fed. Cir. 2006). A mere conclusory statement that one of ordinary skill in the art would have been motivated to combine or modify reference teachings will not suffice. *KSR* at 1396.

The Office has cited several cases, including *Howard v. Detroit Stove Works*, *In re Larsen*, and *In re Fridolph* in support of its 35 U.S.C. § 103(a) rejections of claims 1-33. Each of *Howard v. Detroit Stove Works*, *In re Larsen*, and *In re Fridolph* discusses a situation in which the court held that it would have been obvious for one of ordinary skill in the art to take a prior art structure with multiple pieces and integrate those pieces into a one-piece, or unitary, structure.

In this case, the Office does not rely upon *Howard v. Detroit Stove Works*, *In re Larsen*, or *In re Fridolph* for their law; these cases have been relied upon for the *exact opposite* proposition: that it would have been obvious for one of ordinary skill in the art to take a single-piece structure from the prior art and divide it into multiple regions. Unfortunately, none of *Howard v. Detroit Stove Works*, *In re Larsen*, or *In re Fridolph* supports the Office's proposed interpretation. Nor has the Office cited any law that does support its position. Therefore, the references upon which the Office has based its 35 U.S.C. § 103(a) rejections must be considered for the subject matter that they do or do not disclose.

Foster

Claims 42-44 were rejected under 35 U.S.C. § 103(a) for reciting subject matter that is assertedly unpatentable over the teachings of Foster.

Claims 42-44 are allowable, among other reasons, for depending directly or indirectly from independent claim 19, which is allowable.

Claim 42 is further allowable since Foster does not teach or suggest a semiconductor device structure with a nonconfluent spacer layer that includes a plurality of layers.

Claim 43 depends from claim 42 and is also allowable because Foster does not teach or suggest a nonconfluent spacer layer with one layer that is configured to be secured to an active surface of one semiconductor device and another layer that is configured to be secured to a back side of another semiconductor device.

Claim 44 also depends from claim 42 and is additionally allowable since Foster does not teach or suggest a nonconfluent spacer layer with at least some layers that are at least partially superimposed relative to one another.

Vindasius

Claims 42-44 have been rejected under 35 U.S.C. § 103(a) for being drawn to subject matter that is allegedly unpatentable over the teachings of Vindasius.

Claims 42-44 are allowable, among other reasons, for depending directly or indirectly from independent claim 19, which is allowable.

Claim 43 is also allowable because Vindasius does not teach or suggest a nonconfluent spacer layer with one layer that is configured to be secured to an active surface of one semiconductor device and another layer that is configured to be secured to a back side of another semiconductor device.

Nakanishi in View of Smith

Claims 11 and 12 are rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in Nakanishi, in view of teachings from U.S. Patent 6,049,370 to Smith, Jr. et al. (hereinafter "Smith").

Claims 11 and 12 are both allowable, among other reasons, for depending directly and indirectly, respectively, from independent claim 1, which is allowable.

Nakanishi in View of Blanton

Claim 18 has been rejected under 35 U.S.C. § 103(a) for reciting subject matter which is allegedly unpatentable over the subject matter taught in Nakanishi, in view of teachings from U.S. Patent 5,220,200 to Blanton (hereinafter "Blanton").

Claim 18 is allowable, among other reasons, for depending directly from independent claim 1, which is allowable.

Foster in View of Blanton

Claim 31 stands rejected under 35 U.S.C. § 103(a) for being directed to subject matter that is purportedly unpatentable over the subject matter taught in Foster, in view of teachings from Blanton.

Claim 31 is allowable, among other reasons, for depending directly from independent claim 19, which is allowable.

Vindasius in View of Blanton

Claims 18 and 31 were rejected under 35 U.S.C. § 103(a) for being drawn to subject matter that is assertedly unpatentable over teachings from Vindasius, in view of teachings from Blanton.

Claims 18 and 31 are both allowable, among other reasons, for respectively depending from independent claims 1 and 19, which are allowable.

Nakanishi in View of Mueller

Claims 11 and 13 stand rejected under 35 U.S.C. § 103(a) for being directed to subject matter that is purportedly not patentable over the subject matter taught in Nakanishi, in view of the teachings of U.S. Patent 6,316,786 to Mueller et al. (hereinafter "Mueller").

Claims 11 and 13 both allowable, among other reasons, for depending directly from independent claim 1, which is allowable.

Foster in View of Mueller

Claim 32 stands rejected under 35 U.S.C. § 103(a) for being directed to subject matter that is purportedly not patentable over the subject matter taught in Foster, in view of the teachings of Mueller.

Claim 32 is allowable, among other reasons, for depending directly from independent claim 19, which is allowable.

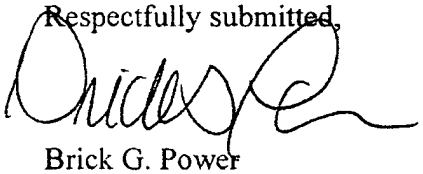
ELECTION OF SPECIES REQUIREMENT

Independent claim 1 remains generic to all of the species of invention that were identified in the Election of Species Requirement in the above-referenced application. In view of the allowability of these claims, claims 14-16, 27-30, 34-36, 41, and 45-67, which have been withdrawn from consideration, should also be considered and allowed. M.P.E.P. § 806.04(d).

CONCLUSION

It is respectfully submitted that each of claims 1-39 and 41-67 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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